Code No: D0603, D7704, D6804, D5704 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012
DESIGN OF FAULT TOLERANT SYSTEMS
(COMMON TO DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Differentiate Reliability and fault tolerance.
b) Why do we need fault-tolerance?
c) Explain fault Tolerant design of memory systems using error correcting codes.

2.a) Define the terms fault-secure and self testing of a circuit.
b) Design a two-level totally self checking checker for m-out-of-(2m+1),m>1. Using reddy's procedure.

3.a) Explain with example OR-AND-OR Design for Testable Combinational logic Circuits.
b) Explain with example Design of Testable Combinational logic Circuits, using control logic.

4.a) Differentiate Scan Based testing and Functional testing.
b) Explain Scan based Design rules (LSSD).

5. Explain Memory Test architecture with example.

6. Distinguish between static and dynamic redundancy.

7. Design fail-safe synchronous sequential machine for a given machine A using Berger codes.
Machine A is:

Present state	Input	
	x=0	x=1
A	E,0	B,0
B	C,0	D,0
C	A,0	D,0
D	E.0	D,1
E	A,0	D,1

8. Write short notes on
a) Discuss with example Design of Testable Combinational logic Circuits, using Syndrome-testable design.
b) Discuss Reliability of series, Parallel and Parallel-Series combinational circuits.

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